

Single channel high-side driver with analog current sense for 24 V automotive applications

Datasheet – production data



- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_{CC}
- Thermal shutdown
- Reverse battery protected with self switch of the PowerMOS
- Electrostatic discharge protection

Features

| | | |
|------------------------------|-----------|--------------------------|
| Max transient supply voltage | V_{CC} | 58V |
| Operating voltage range | V_{CC} | 8 to 36V |
| Typ ON-state resistance | R_{ON} | 16 m Ω |
| Current limitation (typ) | I_{LIM} | 60 A |
| OFF-state supply current | I_S | 2 μ A ⁽¹⁾ |

1. Typical value with all loads connected.

- General
 - Very low stand-by current
 - 3.0 V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - Compliant with European directive 2002/95/EC
 - Fault reset standby pin (FR_Stby)
- Diagnostic functions
 - Proportional load current sense
 - Current sense precision for wide range currents
 - Off-state open load detection
 - Output short to V_{CC} detection
 - Overload and short to ground latch-off
 - Thermal shutdown latch-off
 - Very low current sense leakage
- Protections
 - Undervoltage shutdown

Applications

- All types of resistive, inductive and capacitive loads

Description

The VN5T016AH-E is a device made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes. This device integrates an analog current sense which delivers a current proportional to the load current. Fault conditions such as overload, overtemperature or short to V_{CC} are reported via the current sense pin.

Output current limitation protects the device in overload condition. The device latches off in case of overload or thermal shutdown.

The device is reset by a low level pass on the fault reset standby pin.

A permanent low level on the inputs and fault reset standby pin disables all outputs and sets the device in standby mode.

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1 Block diagram and pin description

Figure 1. Block diagram

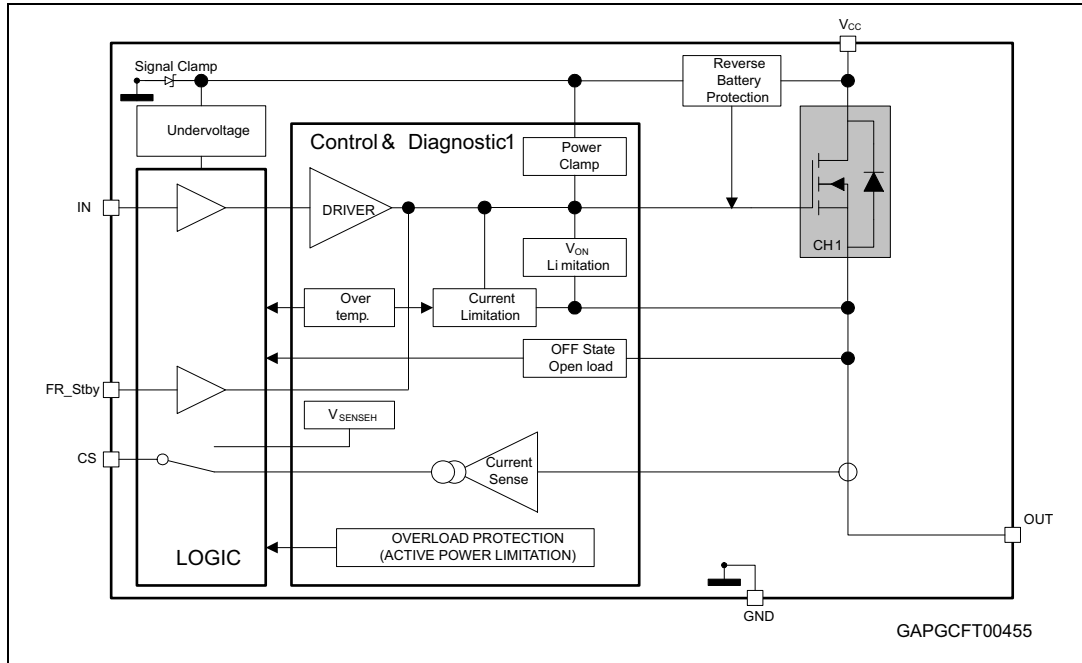


Table 1. Pin function

| Name | Function |
|-----------------|--|
| V _{CC} | Battery connection |
| OUT | Power output |
| GND | Ground connection |
| IN | Voltage controlled input pin with hysteresis, CMOS compatible. It controls output switch state |
| CS | Analog current sense pin, it delivers a current proportional to the load current |
| FR_Stby | In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_Stby pin are low. |

Figure 2. Configuration diagram (top view)

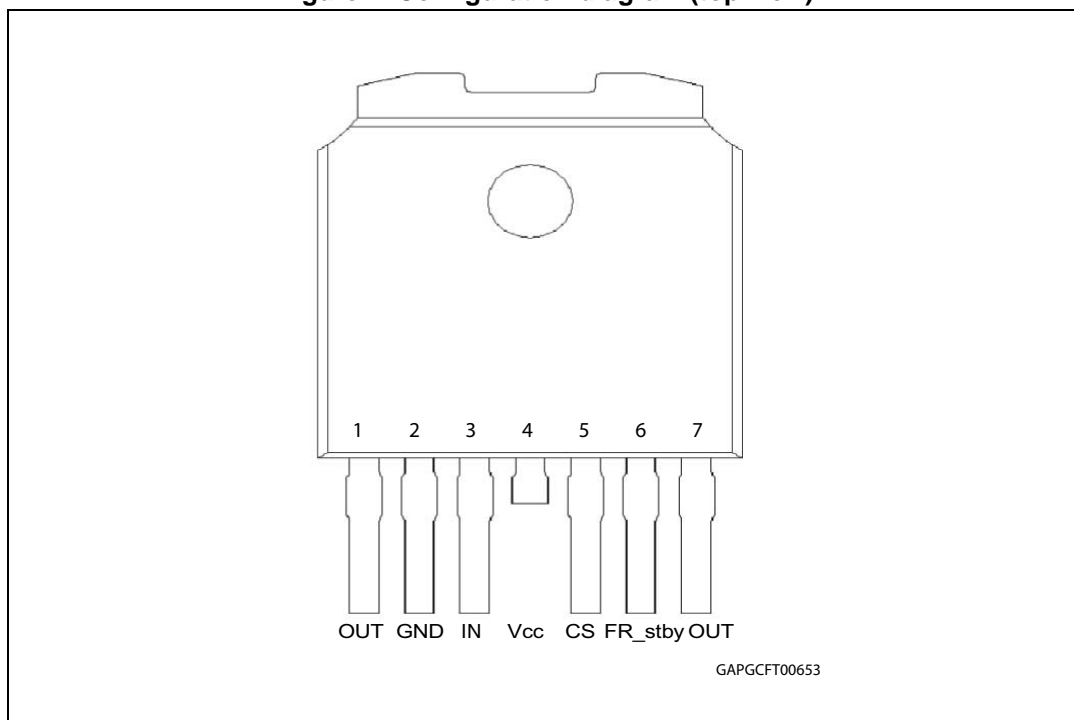


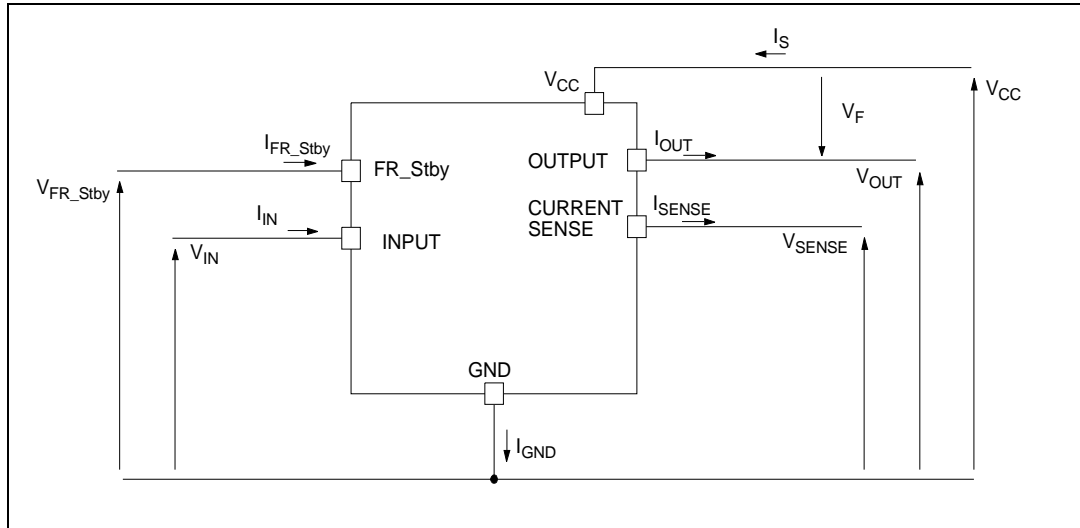
Table 2. Suggested connections for unused and not connected pins

| Connection / pin | Current Sense | N.C. | Output | Input | FR_Stby |
|------------------|------------------------|------------------|-------------|------------------------|------------------------|
| Floating | Not allowed | X ⁽¹⁾ | X | X | X |
| To ground | Through 10 kΩ resistor | X | Not allowed | Through 10 kΩ resistor | Through 10 kΩ resistor |

1. X: do not care.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|----------------------------|---------|
| V_{CC} | DC supply voltage | 58 | V |
| $-V_{CC}$ | Reverse DC supply voltage | -32 | V |
| I_{OUT} | DC output current | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | 30 | A |
| I_{IN} | DC input current | -1 to 10 | mA |
| I_{FR_Stby} | Fault reset standby DC input current | -1 to 1.5 | mA |
| V_{CSense} | Current sense maximum voltage | $V_{CC} - 58$ to $+V_{CC}$ | V |
| E_{MAX} | Maximum switching energy ($L = 10$ mH; $V_{bat} = 32$ V; $T_{jstart} = 150^{\circ}C$; $I_{OUT} = 5.9$ A) | 390 | mJ |
| L_{SMAX} | Maximum stray inductance in short circuit condition ($V_{bat} = 32$ V; $R_L = 300$ m Ω ; $T_{jstart} = 150^{\circ}C$; $I_{OUT} = I_{limH_max}$) | 40 | μ H |

Table 3. Absolute maximum ratings (continued)

| Symbol | Parameter | Value | Unit |
|------------------|---|------------|------|
| V _{ESD} | Electrostatic discharge (Human Body Model: R = 1.5 kΩ; C = 100 pF) | | |
| | – INPUT | 4000 | V |
| | – CURRENT SENSE | 2000 | V |
| | – FAULT RESET STANDBY PIN | 4000 | V |
| | – OUTPUT | 5000 | V |
| | – V _{CC} | 5000 | V |
| V _{ESD} | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| T _j | Junction operating temperature | -40 to 150 | °C |
| T _{stg} | Storage temperature | -55 to 150 | °C |

2.2 Thermal data

Table 4. Thermal data

| Symbol | Parameter | Value | Unit |
|-----------------------|--|-------------------------------|------|
| R _{thj-case} | Thermal resistance junction-case (max.) | 1.5 | °C/W |
| R _{thj-amb} | Thermal resistance junction-ambient (max.) | See Figure 27 | °C/W |

2.3 Electrical characteristics

$8\text{ V} < V_{CC} < 36\text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified.

Table 5. Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------------|---|------|------------------|------|---------------|
| V_{CC} | Operating supply voltage | | 8 | 24 | 36 | V |
| V_{USD} | Undervoltage shutdown | | | 3.5 | 5 | V |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.5 | | V |
| R_{ON} | On-state resistance | $I_{OUT} = 5\text{ A}$; $T_j = 25^\circ\text{C}$; $8\text{ V} < V_{CC} < 36\text{ V}$ | | 16 | | m Ω |
| | | $I_{OUT} = 5\text{ A}$; $T_j = 150^\circ\text{C}$; $8\text{ V} < V_{CC} < 36\text{ V}$ | | | 32 | |
| $R_{ON REV}$ | Reverse battery ON-state resistance | $V_{CC} = -24\text{ V}$; $I_{OUT} = -5\text{ A}$; $T_j = 25^\circ\text{C}$ | | | 16 | m Ω |
| V_{clamp} | Clamp voltage | $I_S = 20\text{ mA}$ | 58 | 64 | 70 | V |
| I_S | Supply current | Off-state; $V_{CC} = 24\text{ V}$; $T_j = 25^\circ\text{C}$; $V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$ | | 2 ⁽¹⁾ | 5 | μA |
| | | On-state; $V_{CC} = 24\text{ V}$; $V_{IN} = 5\text{ V}$; $I_{OUT} = 0\text{ A}$ | | 2.5 | 5 | mA |
| $I_{L(off1)}$ | Off-state output current | $V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 24\text{ V}$; $T_j = 25^\circ\text{C}$ | 0 | 0.01 | 3 | μA |
| | | $V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 24\text{ V}$; $T_j = 125^\circ\text{C}$ | 0 | | 5 | |

1. PowerMOS leakage included.

Table 6. Switching ($V_{CC} = 24\text{ V}$; $T_j = 25^\circ\text{C}$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---|---------------------|------|------|------|------------------|
| $t_{d(on)}$ | Turn-on delay time | $R_L = 4.8\ \Omega$ | — | 55 | — | μs |
| $t_{d(off)}$ | Turn-off delay time | $R_L = 4.8\ \Omega$ | — | 53 | — | μs |
| $dV_{OUT}/dt_{(on)}$ | Turn-on voltage slope | $R_L = 4.8\ \Omega$ | | 0.59 | | V/ μs |
| $dV_{OUT}/dt_{(off)}$ | Turn-off voltage slope | $R_L = 4.8\ \Omega$ | | 0.54 | | V/ μs |
| W_{ON} | Switching energy losses during t_{won} | $R_L = 4.8\ \Omega$ | — | 2.35 | — | mJ |
| W_{OFF} | Switching energy losses during t_{woff} | $R_L = 4.8\ \Omega$ | — | 1.05 | — | mJ |

Table 7. Logic inputs

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|--|---------------------------------------|------|------|------|---------------|
| V_{IL} | Input low level voltage | | | | 0.9 | V |
| I_{IL} | Low level input current | $V_{IN} = 0.9\text{ V}$ | 1 | | | μA |
| V_{IH} | Input high level voltage | | 2.1 | | | V |
| I_{IH} | High level input current | $V_{IN} = 2.1\text{ V}$ | | | 10 | μA |
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.25 | | | V |
| V_{ICL} | Input clamp voltage | $I_{IN} = 1\text{ mA}$ | 5.5 | | 7 | V |
| | | $I_{IN} = -1\text{ mA}$ | | -0.7 | | |
| $V_{FR_Stby_L}$ | Fault reset standby low level voltage | | | | 0.9 | V |
| $I_{FR_Stby_L}$ | Low level fault reset standby current | $V_{FR_Stby} = 0.9\text{ V}$ | 1 | | | μA |
| $V_{FR_Stby_H}$ | Fault reset standby high level voltage | | 2.1 | | | V |
| $I_{FR_Stby_H}$ | High level fault reset standby current | $V_{FR_Stby} = 2.1\text{ V}$ | | | 10 | μA |
| $V_{FR_Stby(hyst)}$ | Fault reset standby hysteresis voltage | | 0.25 | | | V |
| $V_{FR_Stby_CL}$ | Fault reset standby clamp voltage | $I_{FR_Stby} = 15\text{ mA (10 ms)}$ | 11 | | 15 | V |
| | | $I_{FR_Stby} = -1\text{ mA}$ | | -0.7 | | |
| t_{reset} | Overload latch-off reset time | See Figure 4 | 2 | | 24 | μs |
| t_{stby} | Standby delay | See Figure 5 | 120 | | 1200 | μs |

Figure 4. T_{reset} definition

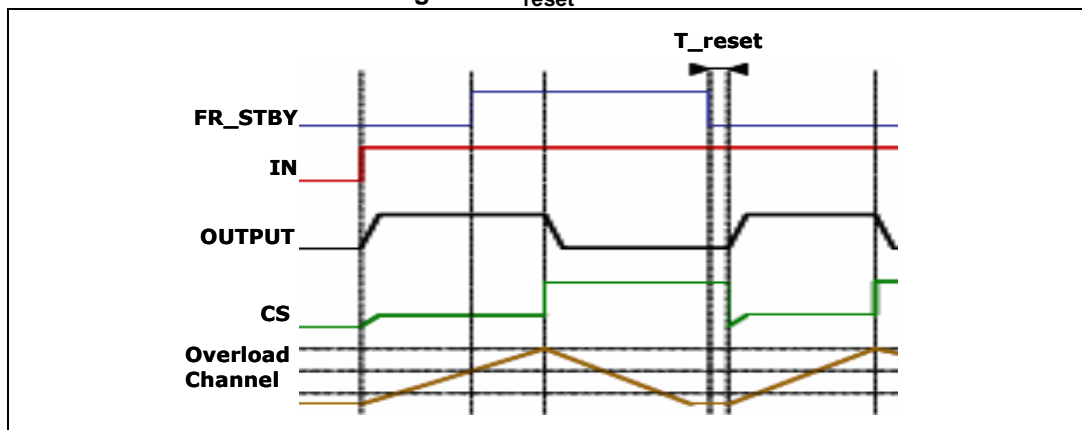


Figure 5. T_{stby} definition

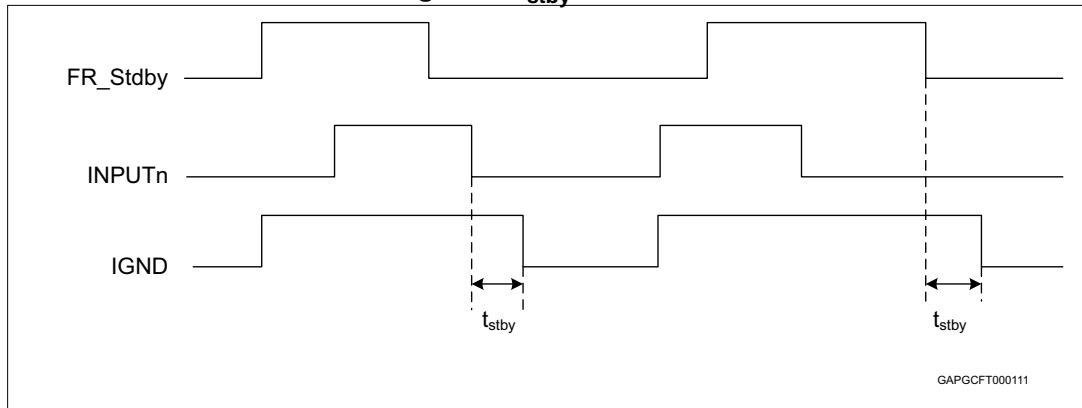


Table 8. Protections and diagnostics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|--|--|-------------|-------------|-------------|--------------------|
| I_{limH} | DC short circuit current | $V_{CC} = 24\text{ V}$ | 43 | 60 | 86 | A |
| | | $5\text{ V} < V_{CC} < 36\text{ V}$ | | | 86 | A |
| I_{limL} | Short circuit current during thermal cycling | $V_{CC} = 24\text{ V}; T_R < T_j < T_{TSD}$ | | 15 | | A |
| T_{TSD} | Shutdown temperature | | 150 | 175 | 200 | $^{\circ}\text{C}$ |
| T_R | Reset temperature | | $T_{RS}+1$ | $T_{RS}+5$ | | $^{\circ}\text{C}$ |
| T_{RS} | Thermal reset of status | | 135 | | | $^{\circ}\text{C}$ |
| T_{HYST} | Thermal hysteresis ($T_{TSD}-T_R$) | | | 7 | | $^{\circ}\text{C}$ |
| V_{DEMAG} | Turn-off output voltage clamp | $I_{OUT} = 5\text{ A}; V_{IN} = 0\text{ V}; L = 6\text{ mH}$ | $V_{CC}-58$ | $V_{CC}-64$ | $V_{CC}-70$ | V |
| V_{ON} | Output voltage drop limitation | $I_{OUT} = 500\text{ mA}; T_j = -40^{\circ}\text{C to } 150^{\circ}\text{C}$ | | 25 | | mV |

Table 9. Current sense ($8\text{ V} < V_{CC} < 36\text{ V}$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|---------------------------|---|--------------|------|--------------|------|
| $dK_{LED}/K_{LED(TOT)}^{(1)}$ | Current sense ratio drift | $I_{OUT} = 12\text{ mA to } 100\text{ mA}; I_{CAL} = 50\text{ mA}; V_{SENSE} = 0.5\text{ V}; T_j = -40^{\circ}\text{C to } 150^{\circ}\text{C}$ | -50 | | 50 | % |
| K_0 | I_{OUT}/I_{SENSE} | $I_{OUT} = 100\text{ mA}; V_{SENSE} = 0.5\text{ V}; T_j = -40^{\circ}\text{C to } 150^{\circ}\text{C}$ | 1333 | 5600 | 11884 | |
| $dK_0/K_0^{(1)}$ | Current sense ratio drift | $I_{OUT} = 100\text{ mA}; V_{SENSE} = 0.5\text{ V}; T_j = -40^{\circ}\text{C to } 150^{\circ}\text{C}$ | -21 | | 32 | % |
| K_1 | I_{OUT}/I_{SENSE} | $I_{OUT} = 0.6\text{ A}; V_{SENSE} = 1\text{ V}; T_j = -40^{\circ}\text{C to } 150^{\circ}\text{C}; T_j = 25^{\circ}\text{C to } 150^{\circ}\text{C}$ | 2418 3139 | 5300 | 9264 7981 | |
| $dK_1/K_1^{(1)}$ | Current sense ratio drift | $I_{OUT} = 0.6\text{ A}; V_{SENSE} = 1\text{ V}; T_j = -40^{\circ}\text{C to } 150^{\circ}\text{C}$ | -21 | | 23 | % |

Table 9. Current sense (8 V < V_{CC} < 36 V) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--|---|---|--------------|------|--------------|------|
| K ₂ | I _{OUT} /I _{SENSE} | I _{OUT} = 1.6 A; V _{SENSE} = 1 V; T _j = -40°C to 150°C T _j = 25 °C to 150 °C | 2928 3072 | 4700 | 7568 6693 | |
| dK ₂ /K ₂ ⁽¹⁾ | Current sense ratio drift | I _{OUT} = 1.6 A; V _{SENSE} = 1 V; T _j = -40°C to 150°C | -26 | | 21 | % |
| K ₃ | I _{OUT} /I _{SENSE} | I _{OUT} = 2.4 A; V _{SENSE} = 2 V; T _j = -40°C to 150°C T _j = 25°C to 150°C | 2912 3007 | 4400 | 7048 6039 | |
| dK ₃ /K ₃ ⁽¹⁾ | Current sense ratio drift | I _{OUT} = 2.4 A; V _{SENSE} = 2 V; T _j = -40°C to 150°C | -19 | | 24 | % |
| K ₄ | I _{OUT} /I _{SENSE} | I _{OUT} = 3 A; V _{SENSE} = 4 V; T _j = -40°C to 150°C T _j = 25 °C to 150 °C | 2843 3142 | 4300 | 6686 5634 | |
| dK ₄ /K ₄ ⁽¹⁾ | Current sense ratio drift | I _{OUT} = 3 A; V _{SENSE} = 4 V; T _j = -40°C to 150°C | -16 | | 22 | % |
| K ₅ | I _{OUT} /I _{SENSE} | I _{OUT} = 4.2 A; V _{SENSE} = 4 V; T _j = -40°C to 150°C T _j = 25°C to 150°C | 3034 3402 | 4250 | 5977 5276 | |
| dK ₅ /K ₅ ⁽¹⁾ | Current sense ratio drift | I _{OUT} = 4.2 A; V _{SENSE} = 4 V; T _j = -40°C to 150°C | -13 | | 16 | % |
| K ₆ | I _{OUT} /I _{SENSE} | I _{OUT} = 20 A; V _{SENSE} = 4 V; T _j = -40°C to 150°C | 3942 | 4240 | 4748 | |
| dK ₆ /K ₆ ⁽¹⁾ | Current sense ratio drift | I _{OUT} = 20 A; V _{SENSE} = 4 V; T _j = -40°C to 150°C | -5 | | 5 | % |
| dK/K _{bulb1(TOT)} ⁽¹⁾ | Current sense ratio drift | I _{OUT} = 1.6 A to 4.2 A; I _{OUTCAL} = 3 A; V _{SENSE} = 4 V; T _j = -40°C to 150°C | -17 | | 40 | % |
| dK/K _{bulb2(TOT)} ⁽¹⁾ | Current sense ratio drift | I _{OUT} = 0.6 A to 2.4 A; I _{OUTCAL} = 1.2 A; V _{SENSE} = 2 V; T _j = -40°C to 150°C | -31 | | 33 | % |
| I _{SENSE0} | Analog sense leakage current | I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{IN} = 0 V; T _j = -40°C to 150°C | 0 | | 1 | μA |
| | | I _{OUT} = 0 A; V _{SENSE} = 0 V; V _{IN} = 5 V; T _j = -40°C to 150°C | 0 | | 2 | |
| V _{SENSE} | Max analog sense output voltage | I _{OUT} = 20 A; R _{SENSE} = 3.9 kΩ | 5 | | | V |
| V _{SENSEH} | Analog sense output voltage in fault condition ⁽²⁾ | V _{CC} = 24 V; R _{SENSE} = 3.9 kΩ | | 8 | | V |
| I _{SENSEH} | Analog sense output current in fault condition ⁽²⁾ | V _{CC} = 24 V; V _{SENSE} = 5 V | | 9 | 12 | mA |

Table 9. Current sense ($8\text{ V} < V_{CC} < 36\text{ V}$) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------------------|--|--|------|------|------|---------------|
| t_{DSENSE2H} | Delay response time from rising edge of INPUT pin | $V_{\text{SENSE}} < 4\text{ V}$; $0.5\text{ A} < I_{\text{OUT}} < 20\text{ A}$; $I_{\text{SENSE}} = 90\%$ of $I_{\text{SENSE max}}$ (see Figure 7) | | 300 | 600 | μs |
| $\Delta t_{\text{DSENSE2H}}$ | Delay response time between rising edge of output current and rising edge of current sense | $V_{\text{SENSE}} < 4\text{ V}$; $I_{\text{SENSE}} = 90\%$ of I_{SENSEMAX} ; $I_{\text{OUT}} = 90\%$ of I_{OUTMAX} ; $I_{\text{OUTMAX}} = 5\text{ A}$ (see Figure 10) | | | 450 | μs |
| t_{DSENSE2L} | Delay response time from falling edge of INPUT pin | $V_{\text{SENSE}} < 4\text{ V}$; $0.5\text{ A} < I_{\text{OUT}} < 20\text{ A}$; $I_{\text{SENSE}} = 10\%$ of $I_{\text{SENSE max}}$ (see Figure 7) | | 3 | 20 | μs |

- Parameter guaranteed by design; it is not tested.
- Fault condition includes: power limitation, overtemperature and open load in OFF-state condition.

Table 10. Open-load detection ($\text{FR_Stby} = 5\text{ V}$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------------|--|---|------|------|------|---------------|
| V_{OL} | Openload off-state voltage detection threshold | $V_{\text{IN}} = 0\text{ V}$; $8\text{ V} < V_{CC} < 36\text{ V}$ | 2 | | 4 | V |
| t_{DSTKON} | Output short circuit to V_{CC} detection delay at turn-off | See Figure 8 | 180 | | 1800 | μs |
| $I_{\text{L(off2)}}$ | Off-state output current at $V_{\text{OUT}} = 4\text{ V}$ | $V_{\text{IN}} = 0\text{ V}$; $V_{\text{SENSE}} = 0\text{ V}$; V_{OUT} rising from 0 V to 4 V | -120 | | 0 | μA |
| $t_{\text{d_vol}}$ | Delay response from output rising edge to V_{SENSE} rising edge in openload | $V_{\text{OUT}} = 4\text{ V}$; $V_{\text{IN}} = 0\text{ V}$; $V_{\text{SENSE}} = 90\%$ of V_{SENSEH} ; $R_{\text{SENSE}} = 3.9\text{ k}\Omega$ | | | 20 | μs |
| $t_{\text{DFRSTK_ON}}$ | Output short circuit to V_{CC} detection delay at FRSTBY activation | See Figure 8 ; Input _{1,2} = low | | | 50 | μs |

Figure 6. Output stuck to V_{CC} detection delay time at FR_{STBY} activation

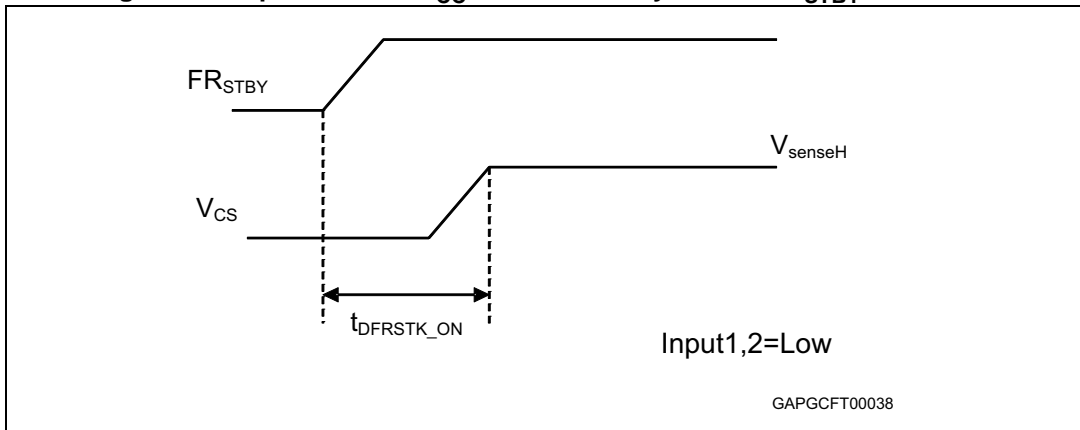


Figure 7. Current sense delay characteristics

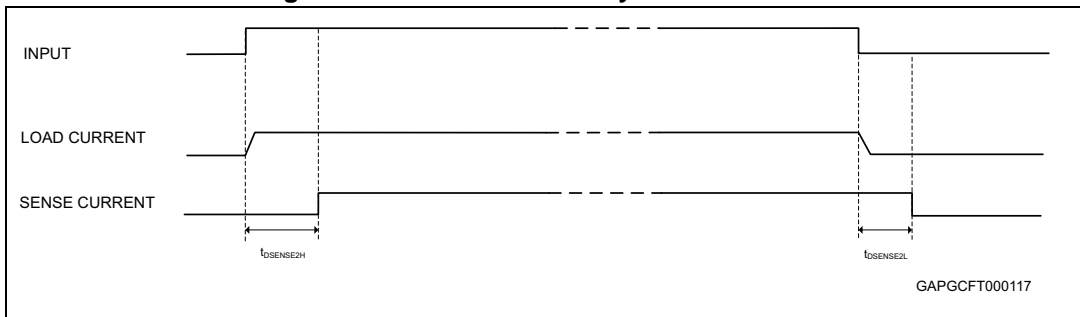
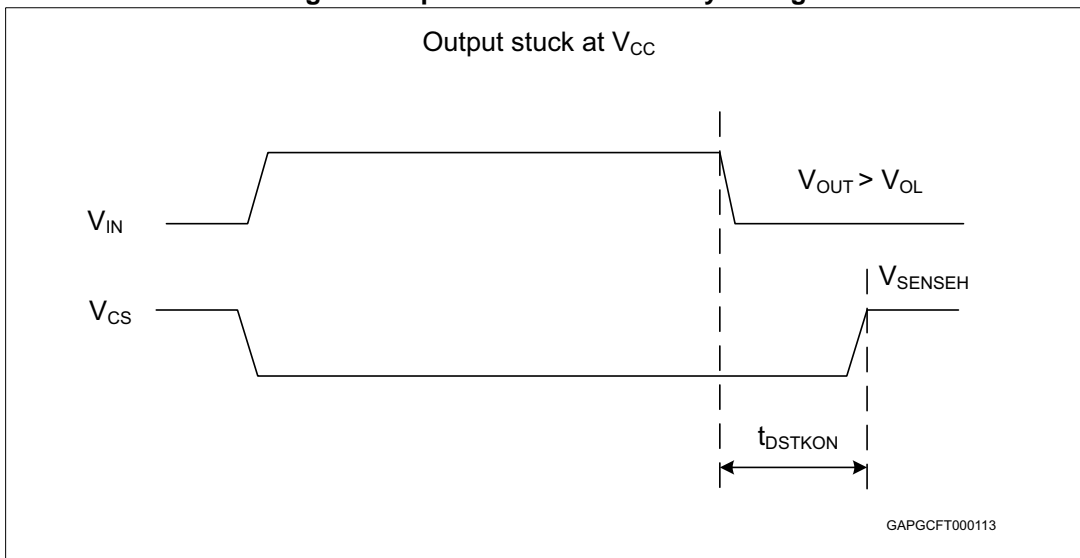


Figure 8. Open-load off-state delay timing



1. With $FR_Stby = 5 V$.

Figure 9. Switching characteristics

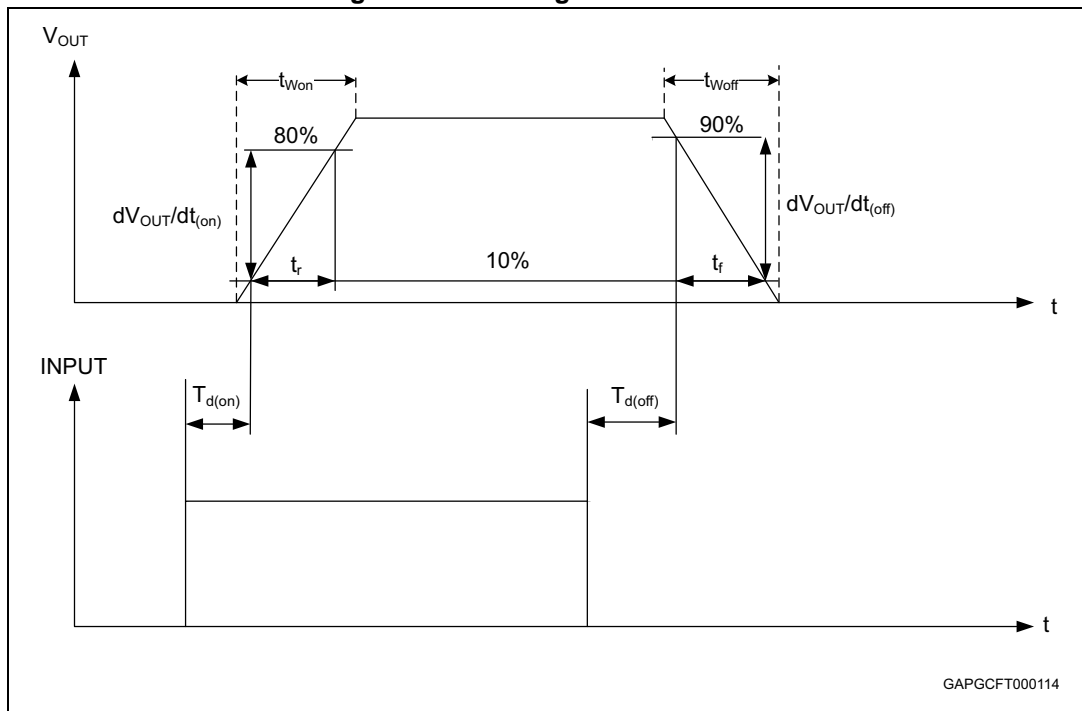


Figure 10. Delay response time between rising edge of output current and rising edge of current sense

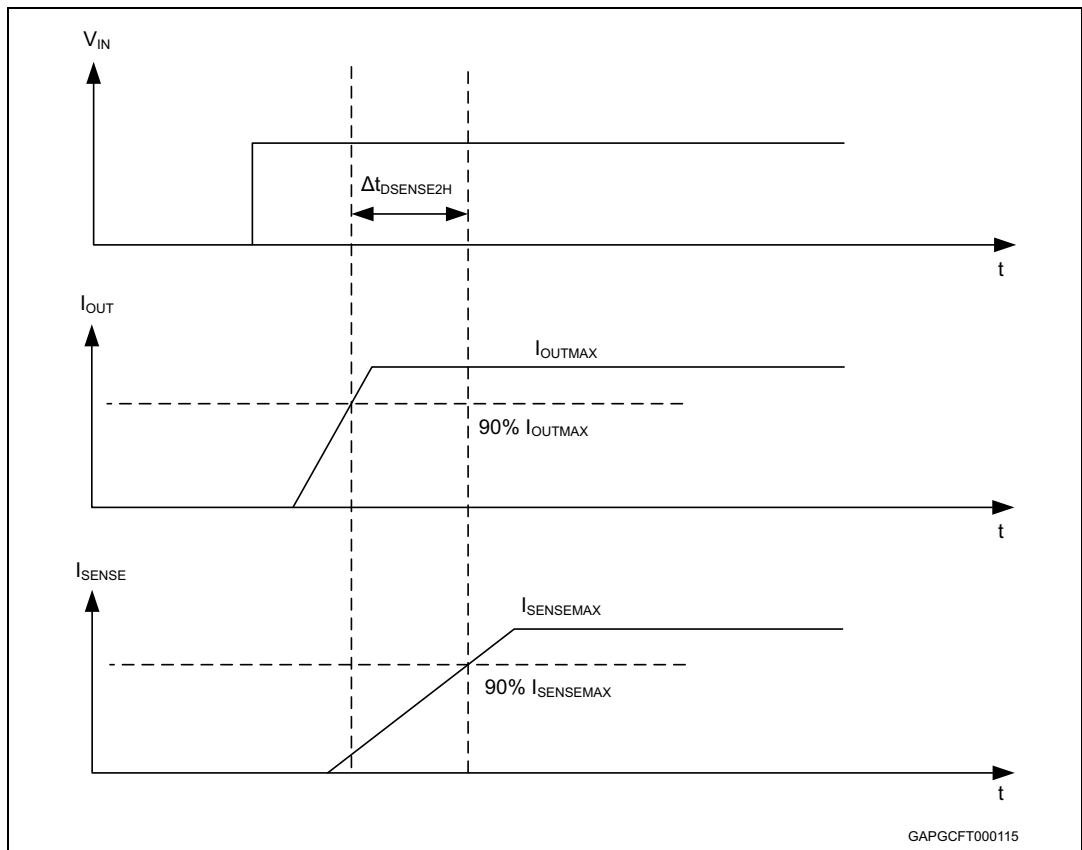


Figure 11. Output voltage drop limitation

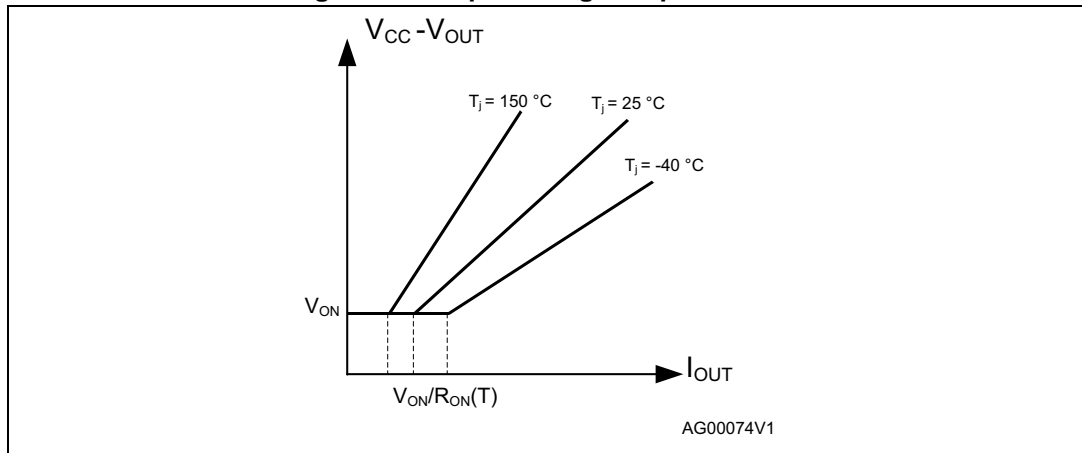


Figure 12. Device behavior in overload condition

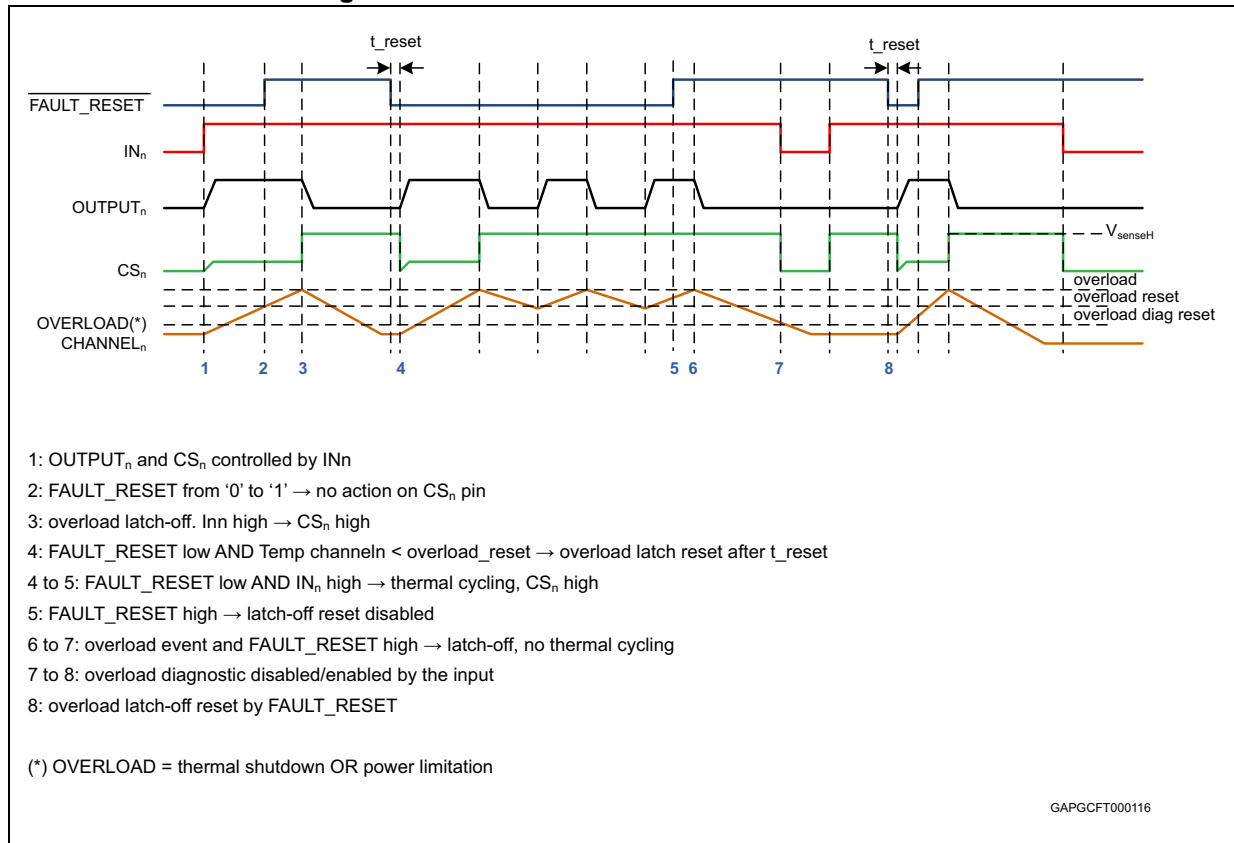


Table 11. Truth table

| Conditions | Fault reset standby | Input | Output | Sense |
|------------------------------------|---------------------|-------|----------|--------------|
| Standby | L | L | X | 0 |
| Normal operation | X | L | L | 0 |
| | X | H | H | Nominal |
| Overload | X | L | L | 0 |
| | X | H | H | > Nominal |
| Overtemperature / short to ground | X | L | L | 0 |
| | L | H | Cycling | V_{SENSEH} |
| | H | H | Latched | V_{SENSEH} |
| Undervoltage | X | X | L | 0 |
| Short to V_{BAT} | L | L | H | 0 |
| | H | L | H | V_{SENSEH} |
| | X | H | H | < Nominal |
| Open load off-state (with pull-up) | L | L | H | 0 |
| | H | L | H | V_{SENSEH} |
| | X | H | H | 0 |
| Negative output voltage clamp | X | L | Negative | 0 |

Table 12. Electrical transient requirements (part 1)

| ISO 7637-2: 2004(E) Test pulse | Test levels ⁽¹⁾ | | Number of pulses or test times | Burst cycle/pulse repetition time | | Delays and impedance |
|--------------------------------------|----------------------------|---------|--------------------------------|-----------------------------------|--------|----------------------|
| | III | IV | | | | |
| 1 | - 450 V | - 600 V | 5000 pulses | 0.5 s | 5 s | 1 ms, 50 Ω |
| 2a | + 37 V | + 50 V | 5000 pulses | 0.2 s | 5 s | 50 μs, 2 Ω |
| 3a | - 150 V | - 200 V | 1h | 90 ms | 100 ms | 0.1 μs, 50 Ω |
| 3b | + 150 V | + 200 V | 1h | 90 ms | 100 ms | 0.1 μs, 50 Ω |
| 4 | - 12 V | - 16 V | 1 pulse | | | 100 ms, 0.01 Ω |
| 5b ⁽²⁾ | + 123 V | + 174 V | 1 pulse | | | 350 ms, 1 Ω |

1. The above test levels must be considered referred to $V_{CC} = 24.5V$ except for pulse 5b
2. Valid in case of external load dump clamp: 58V maximum referred to ground.

Table 13. Electrical transient requirements (part 2)

| ISO 7637-2: 2004(E) Test pulse | Test level results | |
|--------------------------------------|--------------------|------------------|
| | III | IV |
| 1 | C | C ⁽¹⁾ |
| 2a | C | C |
| 3a | C | C |
| 3b ⁽²⁾ | E | E |
| 3b ⁽³⁾ | C | C |
| 4 | C | C |
| 5b ⁽⁴⁾ | C | C |

1. With $R_{load} < 24 \Omega$.
2. Without capacitor between V_{CC} and GND.
3. With 10 nF between V_{CC} and GND.
4. External load dump clamp, 58 V maximum, referred to ground.

Table 14. Electrical transient requirements (part 3)

| Class | Contents |
|-------|--|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

2.4 Electrical characteristics curves

Figure 13. Off-state output current

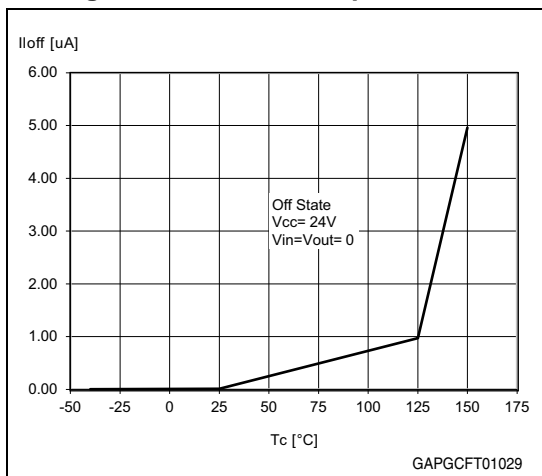


Figure 14. High level input current

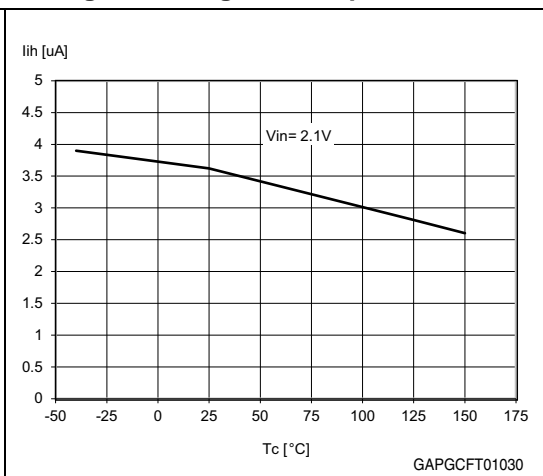


Figure 15. Input clamp voltage

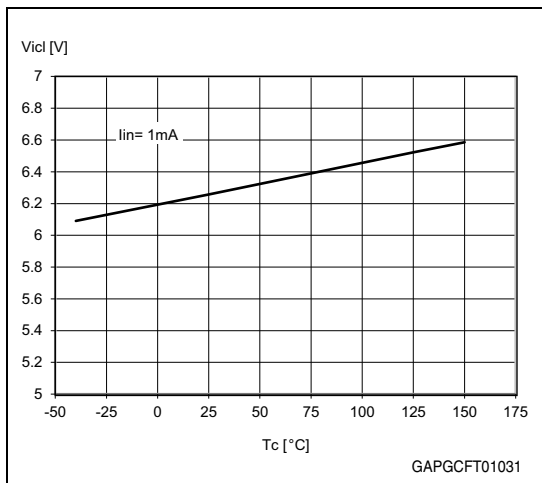


Figure 16. Input low level voltage

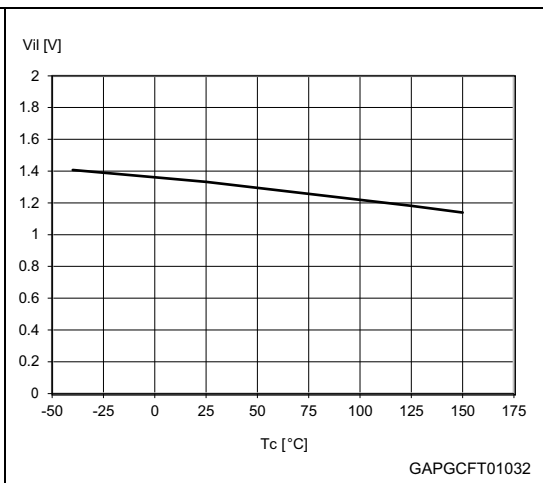


Figure 17. Input high level voltage

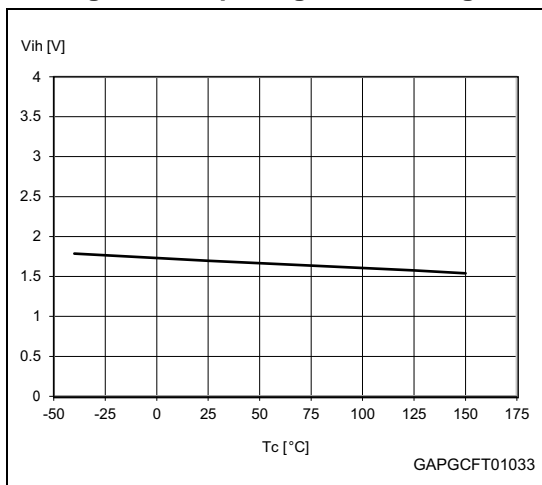


Figure 18. Input hysteresis voltage

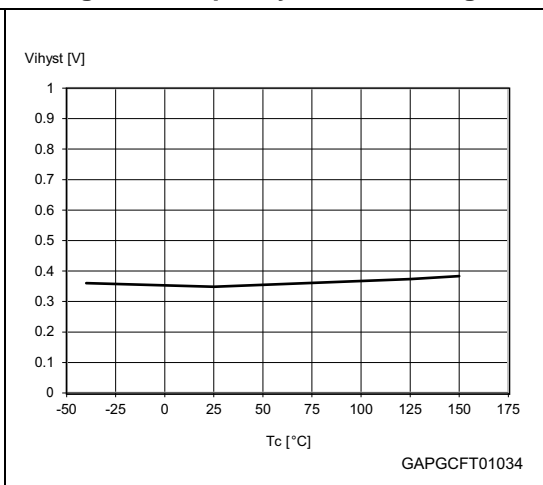


Figure 19. On-state resistance vs T_{case}

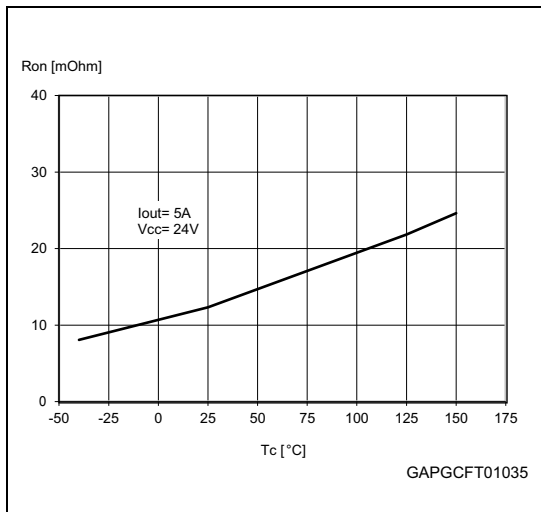


Figure 20. On-state resistance vs V_{CC}

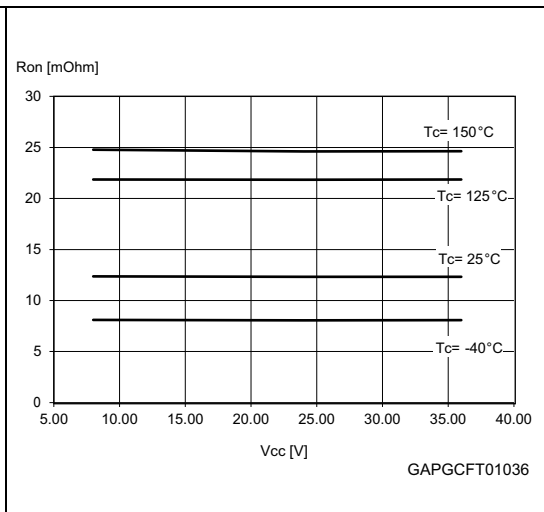


Figure 21. I_{LIMH} vs T_{case}

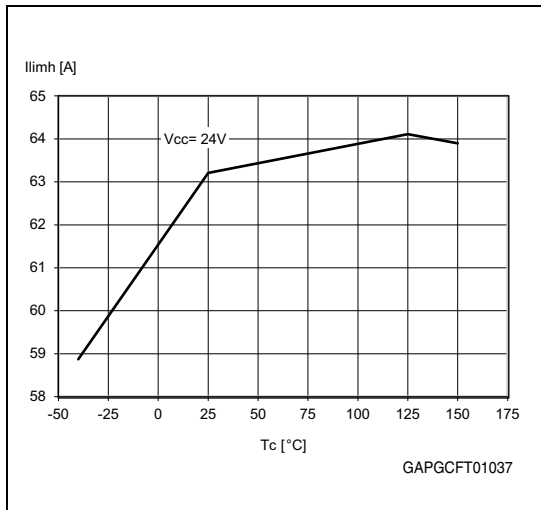


Figure 22. Turn-on voltage slope

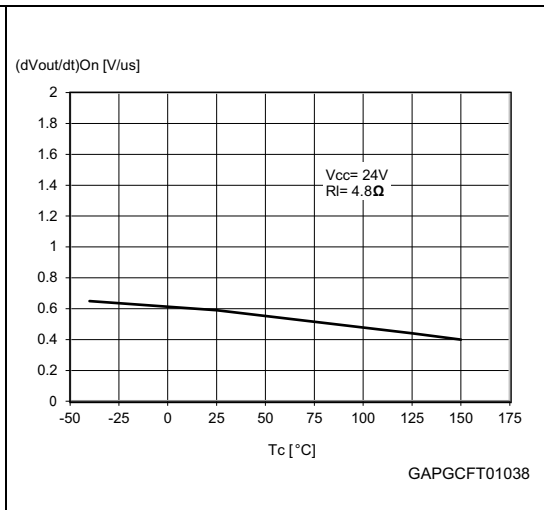
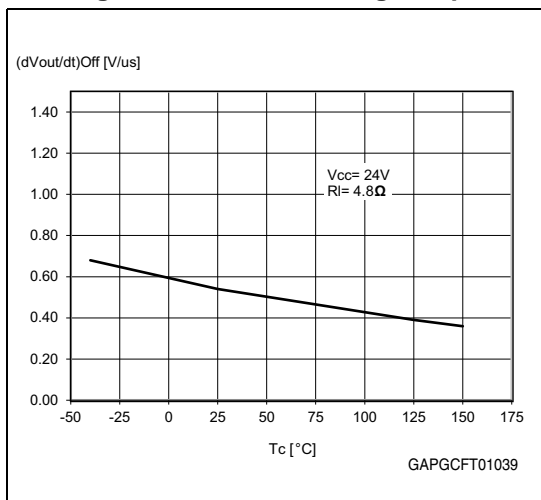
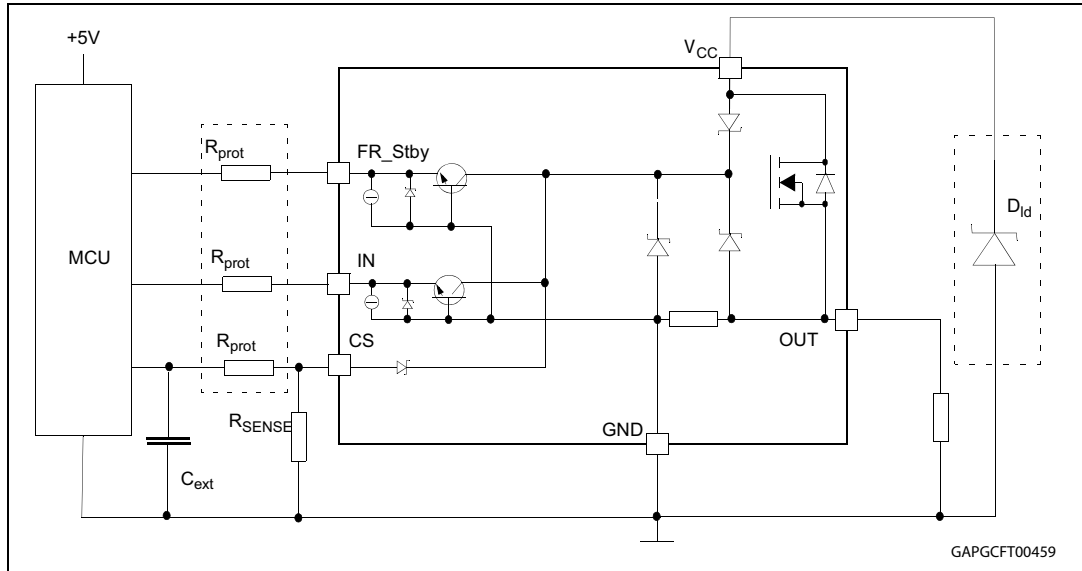


Figure 23. Turn-off voltage slope



3 Application information

Figure 24. Application schematic



3.1 Load dump protection

D_{id} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2 2004 (E) table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins is pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

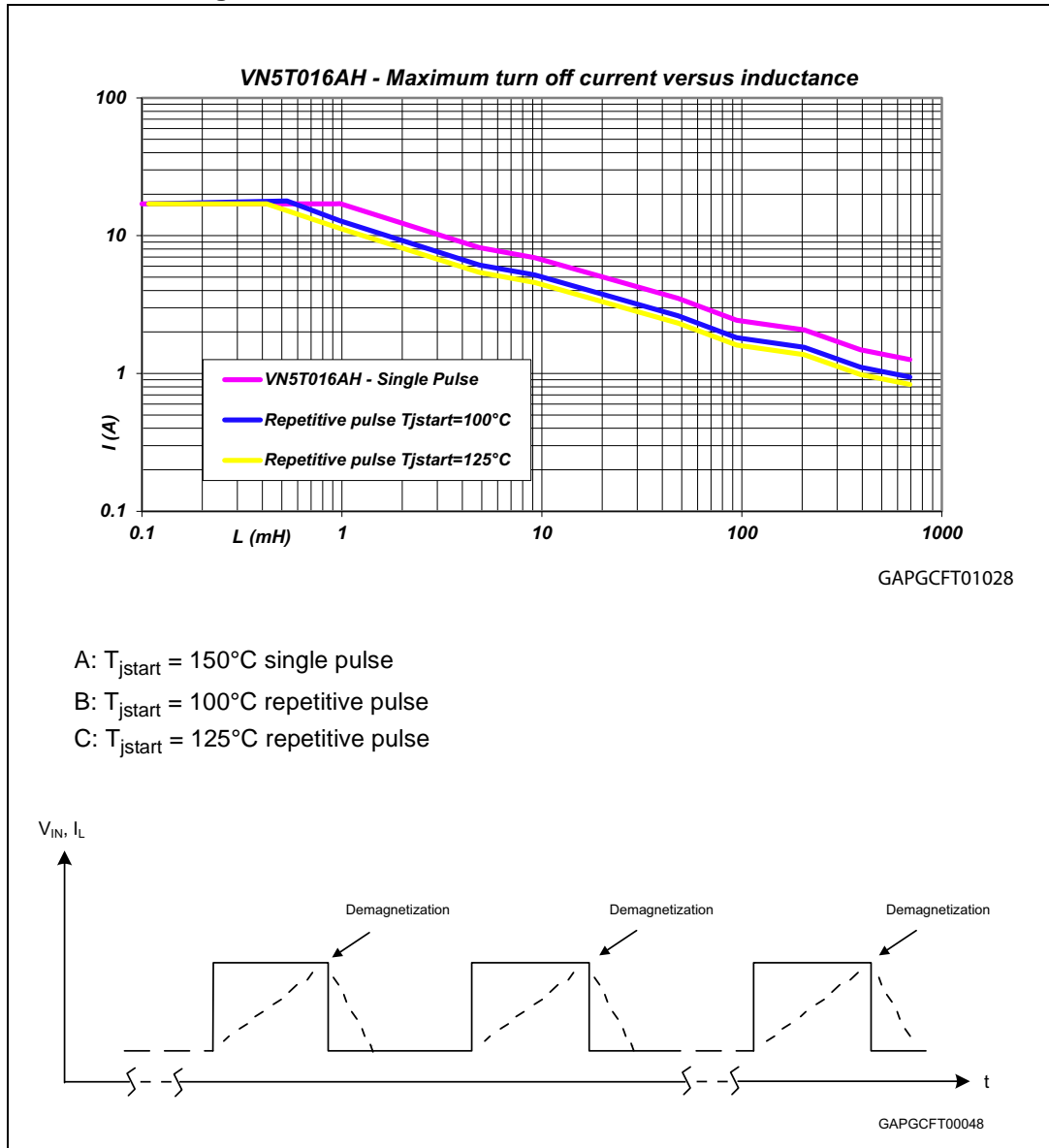
For $V_{CCpeak} = -600$ V and $I_{latchup} \geq 20$ mA; $V_{OH\mu C} \geq 4.5$ V

30 k $\Omega \leq R_{prot} \leq 190$ k Ω .

Recommended value: $R_{prot} = 56$ k Ω

3.3 Maximum demagnetization energy ($V_{CC} = 24\text{ V}$)

Figure 25. Maximum turn-off current versus inductance



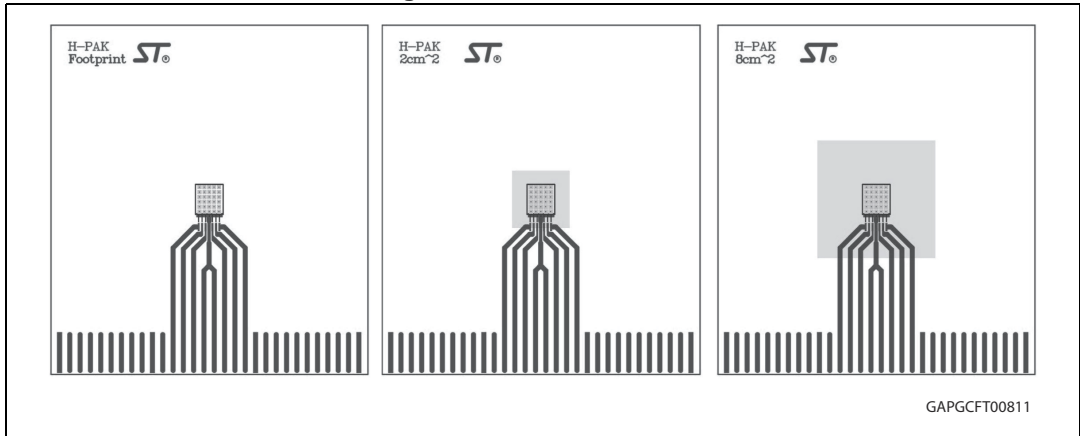
- A: $T_{jstart} = 150^{\circ}\text{C}$ single pulse
- B: $T_{jstart} = 100^{\circ}\text{C}$ repetitive pulse
- C: $T_{jstart} = 125^{\circ}\text{C}$ repetitive pulse

1. Values are generated with $R_L = 0\ \Omega$. In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 HPAK thermal data

Figure 26. HPAK PC board



1. Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 78x86; Board Material FR4; Cu thickness 0.070mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm; Footprint dimension 6.4 mm x 7 mm).

Figure 27. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)

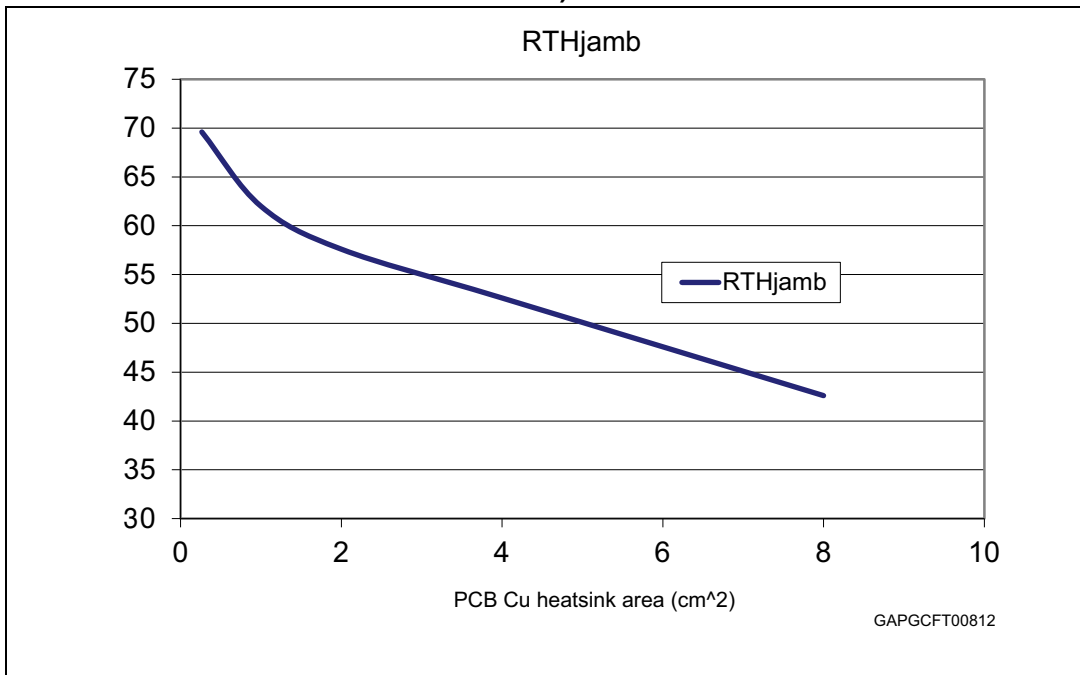


Figure 28. HPAK thermal impedance junction ambient single pulse (one channel ON)

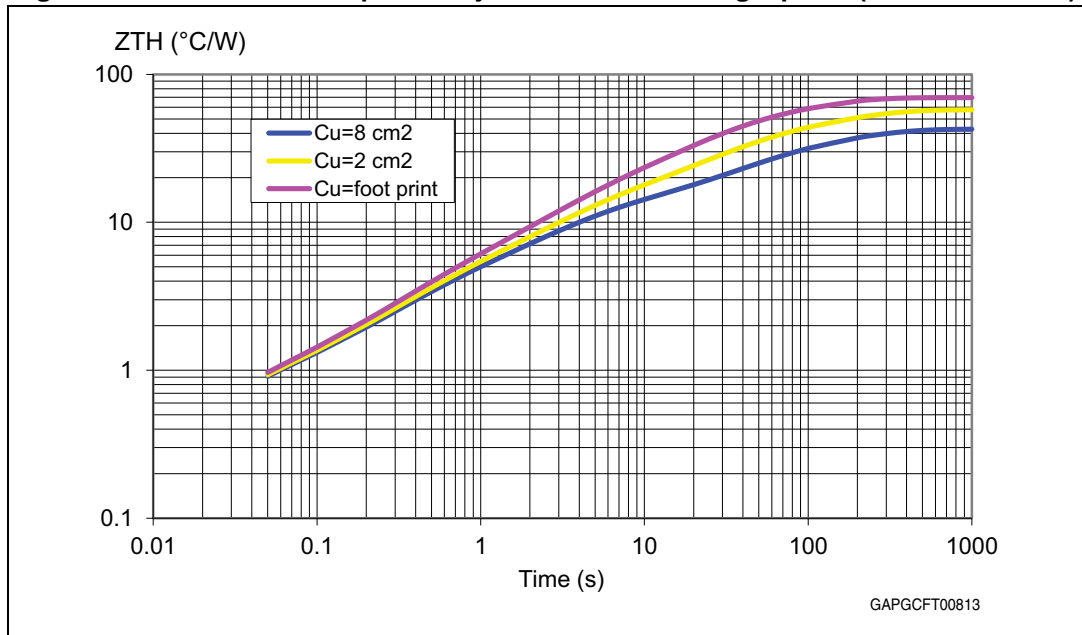
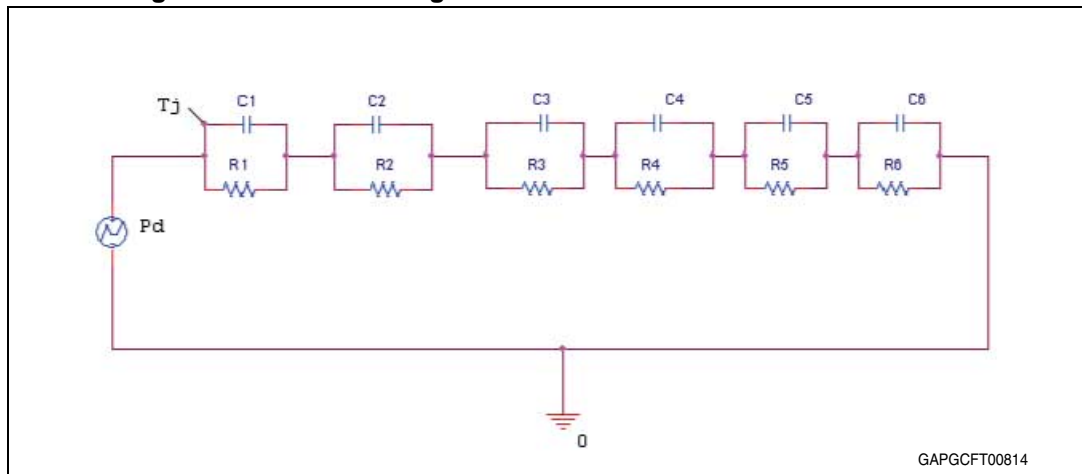


Figure 29. Thermal fitting model of a double channel HSD in HPAK



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 15. Thermal parameters

| Area/island (cm ²) | Footprint | 4 | 8 |
|--------------------------------|-----------|-----|----|
| R1 (°C/W) | 0.1 | | |
| R2 (°C/W) | 0.5 | | |
| R3 (°C/W) | 2 | | |
| R4 (°C/W) | 8 | | |
| R5 (°C/W) | 28 | 22 | 14 |
| R6 (°C/W) | 31 | 25 | 18 |
| C1 (W.s/°C) | 0.01 | | |
| C2 (W.s/°C) | 0.05 | | |
| C3 (W.s/°C) | 0.2 | | |
| C4 (W.s/°C) | 0.4 | | |
| C5 (W.s/°C) | 0.8 | 1.4 | 3 |
| C6 (W.s/°C) | 3 | 6 | 9 |

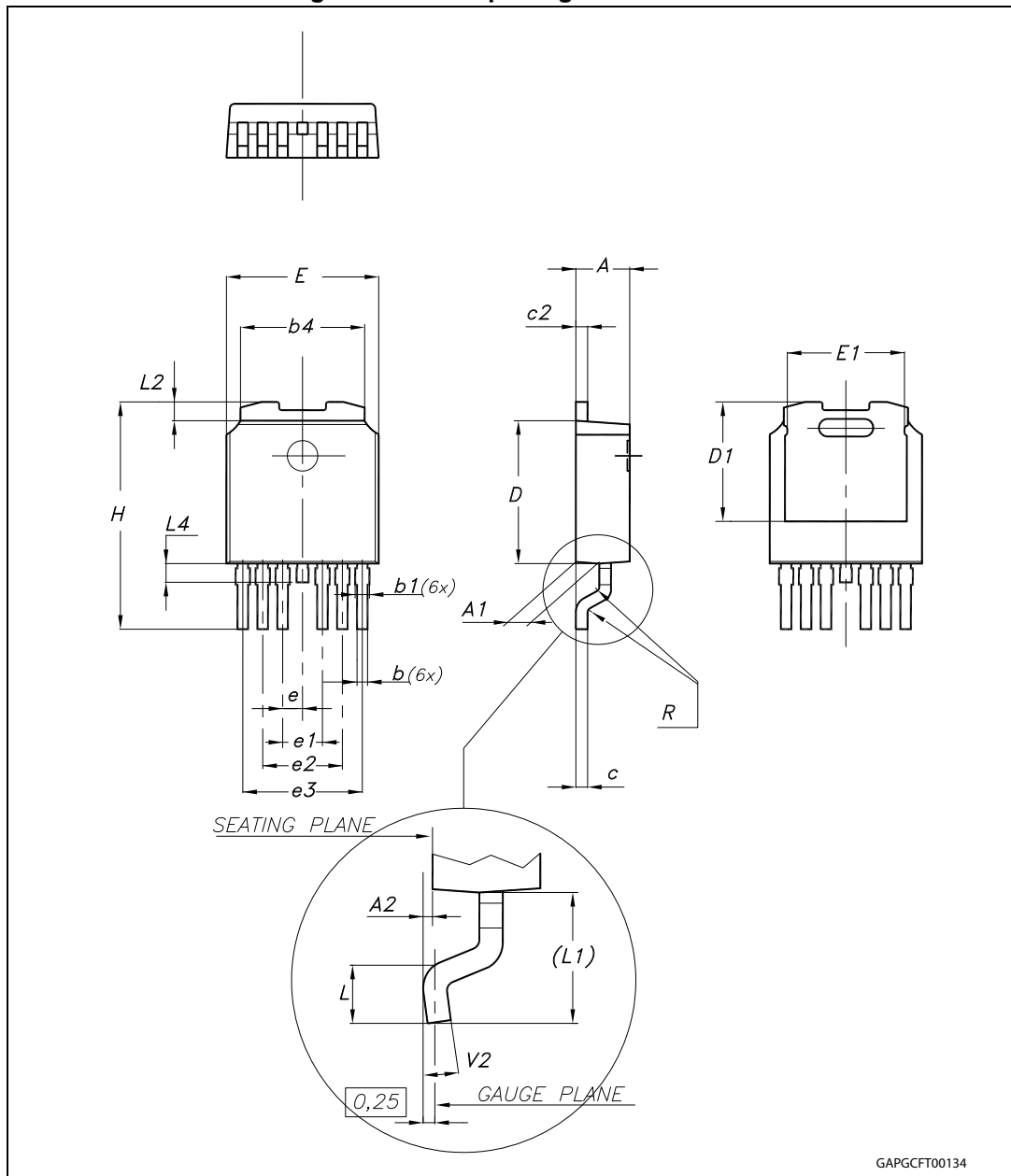
5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.1 HPAK mechanical data

Figure 30. HPAK package dimensions



GAPGCF00134

Table 16. HPAK mechanical data

| Ref. dim | Data book mm | | |
|----------|--------------|------|-------|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.40 | | 0.60 |
| b1 | 0.45 | | 0.65 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | 4.95 | 5.10 | 5.25 |
| E | 6.40 | | 6.60 |
| E1 | 5.00 | 5.20 | 5.40 |
| e | | 0.85 | |
| e1 | 1.60 | | 1.80 |
| e2 | 3.30 | | 3.50 |
| e3 | 5.00 | | 5.20 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | 1.50 |
| (L1) | 2.60 | 2.80 | 3.00 |
| L2 | 0.60 | 0.80 | 1.00 |
| L4 | 0.50 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |

5.2 Packing information

The devices can be packed in tube or tape and reel shipments (see [Table 17: Device summary](#)).

Figure 31. HPAK tube shipment (no suffix)

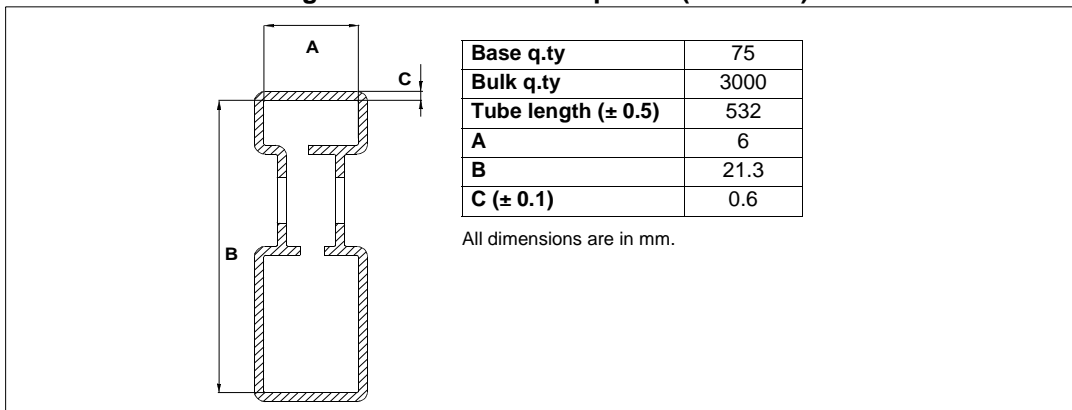
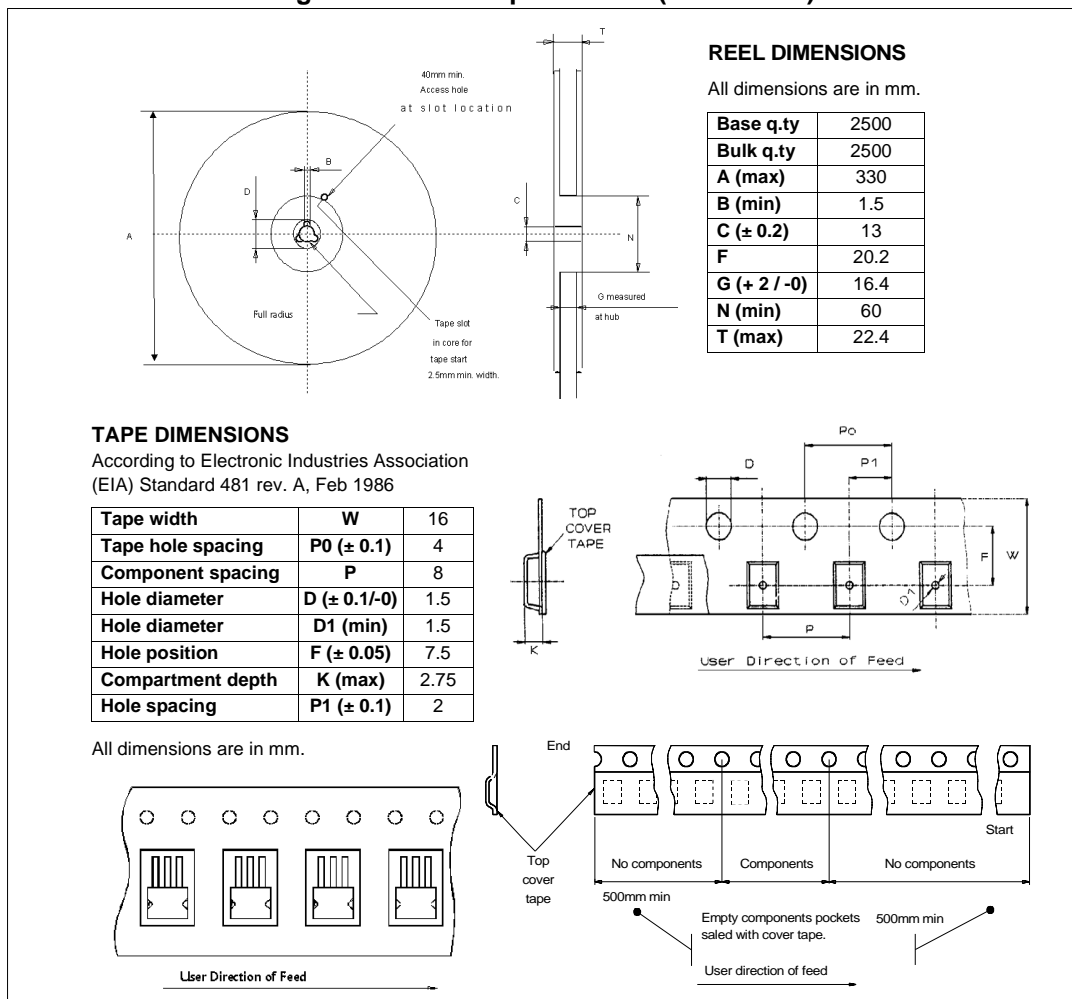


Figure 32. HPAK tape and reel (suffix "TR")



6 Order codes

Table 17. Device summary

| Package | Order codes | |
|---------|-------------|---------------|
| | Tube | Tape and reel |
| HPAK | VN5T016AH-E | VN5T016AHTR-E |

7 Revision history

Table 18. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 01-Oct-2012 | 1 | Initial release. |
| 17-Sep-2013 | 2 | Updated disclaimer. |
| 24-Feb-2016 | 3 | <i>Table 4: Thermal data:</i> – $R_{thj-case}$: updated value Updated <i>Section 5.1: HPAK mechanical data</i> |

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